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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional): MICS:0171-2/MAN/LIU

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on July 28, 2008

Signature /Robert A. Manware/

Typed or printed name Robert A. Manware

Application Number	Filed
10/074,779	February 13, 2002

First Named Inventor: Eric M. Dowling

Art Unit	Examiner
2183	Huisman, David J.

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

- [ ] applicant/inventor.
- [ ] assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)
- [X] attorney or agent of record. Registration number 48,758
- [ ] attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34 _____

/Robert A. Manware/
Signature

Robert A. Manware
Typed or printed name

(281) 970-4545
Telephone number

July 28, 2008
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

[X] *Total of 1 forms are submitted.

This collection of information is required by 35 U.S.C. 132. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11, 1.14 and 41.6. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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PRE-APPEAL BRIEF REQUEST FOR REVIEW

In response to the Final Office Action mailed 5/28/2008 ("Final O.A."), Appellant respectfully submits this Pre-Appeal Brief Request for Review concurrently with a Notice of Appeal regarding the Examiner's improper rejection of claims 1-14, 16-32, 34-47, and 49-50. Because a Notice of Appeal and Pre-Appeal Brief Request for Review was previously submitted on 4/30/2007, resulting in prosecution being reopened by the Panel, Appellants believe that the only fee due at this time is the $10 for the increase in fees for the Notice of Appeal. If, however, this assumption is incorrect, Appellants hereby authorize billing of the entire amount due to the credit card indicated on the attached electronic filing form. In summary, the Examiner rejected all of these claims under Section 103(a) based on a primary reference, Inagami, in combination with one or more additional secondary references. For at least the three reasons set forth below, Appellant submits that all pending claims are in condition for allowance.

1. Register files for loading/storing an *entire* row or selected columns of an *entire* row of a DRAM array in a single operation or in response to a single latch signal.

In the Office Action mailed 8/21/2007, the Examiner asserted that Inagami teaches loading/storing a DRAM row by a register file in response to a single latch signal, a feature generally recited by each of the pending independent claims. *See generally*, Office Action mailed 8/21/2007. Although Appellant did not necessarily agree with these rejections, Appellant amended each of independent claims 1, 13, 16, 23, 28, 46, 49, and 50 in the Response filed 11/21/2007 ("Previous Response") for clarification of certain features. Specifically, each of these claims was amended to clarify that the recited register file loads/stores an entire row (or all selected columns of an entire row) of a DRAM array in a single operation or in response to a single latch signal.

In view of these amendments, Appellant believed that each of the independent claims was clearly distinguishable over Inagami. Specifically, Appellant noted that Inagami, in contrast to the recited subject matter, discloses that at least four operations are required to load/store an entire row of a DRAM into a register file. For instance, as discussed in detail on pp. 30-34 of the Previous Response, Fig. 4 of Inagami illustrates a row 21 (data elements a0-a15) of the main storage 1 (the asserted DRAM array) being loaded into a register file (vector register file 23). As shown in Fig. 4, the vector register file 23 is divided into four storage locations, each having four elements, which the Examiner has correlated with data registers. The four storage locations may be configured to

load data from a row 21 of the main storage 1. For example, depending on the vector mask 22, the first storage location may be configured to load/store elements a0-a3, the second storage location may be configured to load/store elements a4-a7, and so forth. Thus, in order for an entire row of the main storage 21 to be loaded into the register file 23, the first four elements are loaded into the first storage location, the second four elements are loaded into the second storage location, and so forth.

Keeping these points in mind, Inagami also makes it clear that each of the load operations is separate and distinct from the others. For example, Inagami discloses that a first load operation loads vector elements a0-a3 via the load/store sub-pipes 2-0 to 2-3 based on the mask 22 comparison. *See id.* at col. 6, lines 48-63. In a second load operation, vector elements a4 to a7 are compared with the vector mask 22 and loaded accordingly in a similar manner as the first load operation. *See id.* (only elements a4-a6 are loaded due to the masking operation). Similarly, third and fourth load operations follows. *See id.* at col. 6, line 63 to col. 7, line 8. Indeed, Inagami is *explicit* that at least *four* separate operations are required to load an entire row of DRAM (e.g., row 21) into the vector register file 23, which the Examiner asserted as the recited register file.

Appellant further notes that Fig. 5 of Inagami shows a similar technique for executing a series of store operations (essentially the reverse of the load operations described in Fig. 4), wherein data from the vector register 32 is stored into a row 21 of the main storage 1 (designated by vector data structure 12) by four separate and distinct store operations. *See id.* at col. 7, lines 14-36; Fig. 5. Thus, in stark contrast to the recitations of claims 1, 13, 16, 23, 28, 46, 49, and 50, which *clearly* require a register file being capable of loading or storing an *entire* row of DRAM in a single operation, Inagami requires a *plurality* of separate and distinct operations for loading and storing a DRAM row to a register file. Still further, Appellant submits that because Inagami requires at least four load/store operations, separate latch signals would be required for *each* operation. Accordingly, Inagami also fails to teach that an entire row of the DRAM is loaded into a register file in response to a single latch signal. Moreover, even if it could be argued that the multiple load operations taught by Inagami occur in parallel (at the same time), the loading of the row data 21 into vector register files is still four *separate* operations. As such, Appellant submits that no reasonable interpretation of Inagami discloses register files capable of loading or storing an entire row of a DRAM array in a single operation or via a single latch signal.

In the Final O.A., the Examiner acknowledged this deficiency with regard to Inagami, but alleged that Appellant is interpreting the recitation "entire row" too broadly. *See* Final O.A., p. 53.

Specifically, the Examiner stated that "[Appellant], when applying such an interpretation, does make a valid argument." *Id.* The Examiner, however, further insisted that "entire row" should be interpreted to mean a subset of the row 21, or even an individual element or cell. *See id.* Specifically, the Examiner stated:

> ...a single DRAM array row may correspond to a single entry shown in storage 21 in Fig. 4. For instance, data a0 is in row 0, data a1 is in row 1, etc. Or, in an alternate interpretation, a single DRAM row may correspond to four consecutive entries shown in storage 21 in Fig. 4. A row is merely a number of items arranged in a line. Hence, any number of data items in storage 21 can be called a row.

Id. Appellant strongly disagrees and asserts that this proposed interpretation is blatantly inconsistent with the meaning that one skilled in the art would understand the term "entire row" to mean when applied to memory devices. That is, the term "row" has a very specific meaning when used in the context of memory devices, which are typically constructed as an array of storage elements arranged in both a horizontal and vertical manner, generally referred to as rows and columns, respectively. As the Panel will appreciate, a "row" is thus generally regarded as being *all* of the elements within a horizontal row of a memory array. Further, as noted above, Appellant specifically amended each of the independent claims to specify that an entire row is loaded/stored by the register files. Certainly, one skilled in the art would not interpret "entire row" as being either a single memory cell within a row, or a subset of a row.

Therefore, because the Examiner's only rationale for maintaining this rejection is based on the assumption that an "entire row" could mean a single cell within a row, or a subset of cells in a row, and because this assumption is clearly erroneous, Appellant respectfully submits to the Panel that Inagami does not teach or suggest at least this recited feature of claims 1, 13, 16, 23, 28, 46, 49, and 50. As such, each of these claims is believed to be allowable over the cited references.

2. Dual port register files.

In addition, independent claims 23, 45, and 50 each generally recite dual port register files having: (1) a first port operative to parallely transfer contents of a selected register file between a DRAM row; and (2) at least a second port operative to transfer data between the selected file register and functional unit. *See* Application, Fig. 2 (noting that the switches 204 provide dual port connections to a DRAM row 208 and a functional unit 128)

The Examiner asserted the main storage 1, the load/store sub-pipes 2, and the vector registers VR0-VR7, as being the recited DRAM, functional unit, and dual port register files, respectively. Assuming such a correlation is proper, Appellant notes that Inagami clearly does not show that the vector registers VR0-VR7 are configured such that data may be transferred between a (1) register file and the main storage 1 via a first port, and (2) between a register file and a load/store sub-pipe 2 by a second port. Rather, Appellant notes, by way of example, that the main storage 1 is coupled to the load/store sub-pipe 2, which is coupled to the vector register file VR0 by a switch 120. In other words, Inagami clearly shows that the asserted register file, functional unit, and DRAM are connected in series. Thus, as discussed in detail on pp. 27-30 of the Previous Response, any data transferred to or from the main storage 1 to the vector registers VR0-VR7 must pass through the same access port (e.g., switch 120) connecting the load/store sub-pipes 2 to the vector registers VR0-VR7. In other words, Inagami only discloses a single access port for transferring data to the main storage 1 *through* the load/store sub-pipes 2. It does not, as the Examiner suggests, disclose two distinct access ports for transferring data between the main storage 1 and the load/store sub-pipes 2, respectively, as recited by claims 23, 45, and 50.

In the Final O.A., the Examiner further asserted that the switch 273, which is also coupled to the register file VR0, could be considered a second access port. *See* Final O.A., p. 52. However, even if the switch 273 could be considered as a second access port, claims 23, 45, and 50 require not only that the recited register files include two ports, but that a first port is configured to transfer data between a register file and a DRAM, and that a second port is configured to transfer data between a register file and a functional unit. Here, the switch 273 appears to be configured to transfer data to an operation sub-pipe 5. Based on the Examiner's interpretation of Inagami, however, the operation sub-pipe 5 is neither a DRAM nor a functional unit. As such, claims 23, 45, and 50 are believed to be allowable for at least this additional reason.

3. Command to deactivate a row after it has been precharged.

Claim 1 also recites an instruction set including a command to deactivate a row of DRAM after it has been precharged. During prosecution, the Examiner admitted that Inagami fails to disclose this feature, but alleged that Farmwald (in combination with Inagami) discloses a refresh command, which the Examiner equated as being a deactivate command. The Examiner's basis for equating a DRAM refresh operation with the "deactivate command" is that during a refresh, the cell

being refreshed is inaccessible and, therefore, "deactivated" because reads and writes cannot occur. This assumption is clearly erroneous. As discussed in detail on pp. 36-40 of the Previous Response, those skilled in the art will appreciate that a refresh command essentially reads the contents of a memory cell, and then writes the contents back into the *same* memory cell to replenish the charge stored within the cell. In other words, a refresh command consists of both a read and a write operation. To the extent that the Examiner's reliance on Farmwald has any basis whatsoever, it is that a refresh cycle must complete its *own* read and write operations before subsequent read or write operations may be performed. Even so, Appellant submits that those skilled in the art would not equate a refresh command as being the same as a deactivate command.

In the Final O.A., the Examiner acknowledged these points but asserted that the read/write performed during a refresh is *not* part of the program code, and thus during a refresh, program code cannot access the memory. *See* Final O.A., p. 54. However, Appellant notes that the "deactivate command" is clearly recited by claim 1 as being part of the instruction set, and thus *is* part of the program code. Therefore, because the Examiner's rationale for maintaining the present rejection is further based on the assumption that the recited deactivate command is *not* part of the program code, and because this assumption is clearly erroneous, Appellant submits that independent claim 1 is further allowable for this additional reason.

Conclusion

For one or more of the reasons discussed above, all pending independent claims and their respective dependent claims are believed to be allowable over the cited references. If the Panel believes certain amendments are necessary to clarify the present claims or if the Panel wishes to resolve any other issues by way of a telephonic conference, they are kindly invited to contact the undersigned attorney at the telephone number indicated below.

Respectfully submitted,

Date: July 28, 2008

/Robert A. Manware/
Robert A. Manware
Reg. No. 48,758
FLETCHER YODER
(281) 970-4545